CLAIM AMENDMENTS

1. (Currently Amended) A system comprising:

a first transmitter to receive an input signal and to transmit a test signal based on the input signal to a network;

a first receiver to receive a return signal from the network;

a second receiver to receive the test signal from the network; and

a second transmitter to receive the test signal from the second receiver using a serial communications line, wherein the second transmitter is to reduce jitter in the test signal and provide the jitter reduced test signal as the return signal to the first receiver and wherein the second transmitter is to reduce jitter in the test signal based on clock signals provided by a plurality of clock sources and wherein the second transmitter comprises a de-multiplexer to de-serialize the test signal based on the plurality of clock signals.

2. (Previously Presented) The system of Claim 1, further comprising a data processor to provide the input signal to the first transmitter and to receive the return signal from the first receiver, wherein the first receiver is to transfer the return signal with substantially no additional jitter correction to the data processor and wherein the data processor is to determine path integrity characteristics based on the input signal and return signal.

Claims 3 – 5 (Cancelled)

6. (Original) The system of Claim 2, further comprising an interface to exchange signals with the data processor.

7. (Original) The system of Claim 6, wherein the interface is compatible with XAUI.

8. (Original) The system of Claim 6, wherein the interface is compatible with IEEE 1394.

9. (Original) The system of Claim 6, wherein the interface is compatible with PCI.

10. (Original) The system of Claim 6, further comprising a switch fabric coupled to the interface.

11. (Original) The system of Claim 6, further comprising a packet processor coupled to the interface.

12. (Original) The system of Claim 6, further comprising a memory device coupled to the interface.

13. (Original) The system of Claim 2, wherein the data processor is to perform media access control in compliance with IEEE 802.3.

14. (Original) The system of Claim 2, wherein the data processor is to perform optical transport network de-framing in compliance with ITU-T G.709.

15. (Original) The system of Claim 2, wherein the data processor is to perform forward error correction processing in compliance with ITU-T G.975.

16. (Previously Presented) The system of Claim 1, further comprising a data processor to provide the input signal to the first transmitter and wherein the first receiver is to receive the test signal from the first transmitter using a serial communications line and wherein the first receiver is to transfer the test signal with substantially no additional jitter correction to the data processor and wherein the data processor is to determine path integrity characteristics based on the test signal and the input signal.

Claims 17 -19 (Cancelled)

20. (Original) The apparatus of Claim 1, wherein the network comprises an optical network.

21. (Previously Presented) The apparatus of Claim 1, wherein the network includes a copper network with capability to transmit and receive at least at a gigabit per second and in accordance with Ethernet.

Claims 22-25 (Cancelled)

26. (Original) The system of Claim 1, wherein the first transmitter comprises:

a clock and multiplication unit to provide a first clock signal, wherein the first clock signal is based on a phase comparison between a second clock signal and a divided down version of the first clock signal;

a phase detector to selectively provide samples of the input signal based on a third clock signal, wherein the third clock signal is based on the first clock signal;

a de-multiplexer to convert the samples into parallel format based on a divided down version of the third clock signal; and

a second clock source to provide the second clock signal, wherein the second clock signal is based on a phase comparison between the divided down version of the first clock signal and the divided down version of the third clock signal.

27. (Currently Amended) The system of Claim [[1]] 26, wherein the first transmitter further comprises:

a serializer to convert the parallel format samples into serial format samples based on the divided down version of the first clock signal; and

a re-timer to provide the serial format samples from the serializer as the test signal based on the first clock signal.

28. (Original) The system of Claim 1, wherein the first receiver further comprises:

logic to transfer the return signal with substantially no additional jitter correction.

29. (Currently Amended) The system of Claim 1, wherein the second transmitter comprises ~~plurality of clock sources comprise~~:

a clock and multiplication unit to provide a first clock signal, wherein the first clock signal is based on a phase comparison between a second clock signal and a divided down version of the first clock signal;

a phase detector to selectively provide samples of the test signal based on a third clock signal, wherein the third clock signal is based on the first clock signal;

~~a de-multiplexer to convert the samples into parallel format based on a divided down version of the third clock signal;~~ and

a second clock source to provide the second clock signal, wherein the second clock signal is based on a phase comparison between the divided down version of the first clock signal and the divided down version of the third clock signal, wherein the de-multiplexer is to convert the samples into parallel format based on a divided down version of the third clock signal.

30. (Original) The system of Claim 29, wherein the second transmitter comprises:

a serializer to convert the parallel format samples into serial format samples based on the divided down version of the first clock signal; and

a re-timer to provide the serial format samples from the serializer as the return signal based on the first clock signal.

31. (Original) The system of Claim 1, wherein the second receiver is to transfer the test signal with substantially no additional jitter correction to the second transmitter.

32. (Currently Amended) A method comprising:

at a first transceiver:

receiving an input signal, and

transmitting a test signal to a network, wherein the test signal is based on the input signal;

at a second transceiver:

receiving the test signal from the network,

serially transferring the test signal with substantially no additional jitter correction as a first signal,

reducing jitter in the first signal, wherein the reducing jitter includes de-serializing the first signal based on a plurality of clock signals ~~using clock signals from a plurality of clock sources~~,

transmitting the jitter reduced first signal as a second signal to a network; and

at the first transceiver:

receiving the second signal from the network.

33. (Original) The method of Claim 32, further comprising: at the first transceiver, determining path integrity characteristics based on the input signal and the second signal.

34. (Original) The method of Claim 32, wherein at the first transceiver, transmitting the test signal to the network comprises:

reducing jitter in the input signal; and

providing the jitter reduced input signal as the test signal.

35. (Original) The method of Claim 32, further comprising:

at the first transceiver:

determining path integrity characteristics based on a comparison between the input signal and the test signal.

36. (New) An apparatus comprising:

a clock and multiplication unit to provide a first clock signal, wherein the first clock signal is based on a phase comparison between a second clock signal and a divided down version of the first clock signal;

a phase detector to selectively provide samples of an input signal based on a third clock signal, wherein the third clock signal is based on the first clock signal;

a de-multiplexer to convert the samples into parallel format based on a divided down version of the third clock signal;

a second clock source to provide the second clock signal, wherein the second clock signal is based on a phase comparison between the divided down version of the first clock signal and the divided down version of the third clock signal;

a serializer to convert the parallel format samples into serial format samples based on the divided down version of the first clock signal; and

a re-timer to provide the serial format samples from the serializer based on the first clock signal.

37. (New) The apparatus of Claim 36, further comprising:

a data processor to determine path integrity characteristics based on the input signal and a signal based on the serial format samples.

38. (New) The apparatus of Claim 36, further comprising:

a data processor to determine path integrity characteristics based on the input signal and a signal received from a network and based on the serial format samples.